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process illustrated in Figure 21 may be implemented in a data cache <u>unit</u>, such as data cache <u>unit</u> 216 and instruction cache <u>unit</u> 214 in Figure 2.

At page 46, paragraph 1:

With reference next to Figure 22, a diagram illustrating components used in accessing information collected with respect to the execution of instructions or the access of memory locations in accordance with a preferred embodiment of the present invention. In this example, instruction unit 2200 executes instruction 2202 and increments counter 2204. This counter is incremented each time instruction 2202 is executed. In this example, instruction unit 2200 may be implemented as instruction cache unit 214 in Figure 2.

At page 46, last paragraph:

When the instruction or data cache <u>unit</u> pages are loaded into memory, the operating system program loader/linker and/or the performance monitoring program, reads the meta data generated by the compiler and determines that counting is associated with instruction or data access, then the loading process allocates data areas to maintain the counters as part of its perfinst segment. The size of the counters and the granularity of the data access determine the amount of work area to be allocated.

At page 62, last paragraph:

Data accesses may be monitored in a similar fashion. For example, data 3112 includes data range 3114. Data accesses to data range 3114 may be counted in a similar fashion to execution of instructions within instruction range 3102 or instruction range 3104. These ranges may be defined in registers within a data unit, such as data cache <u>unit</u> 216 in Figure 2. These ranges for data may be defined in the register as a range of memory locations for the data.

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At page 48, paragraph 1.

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Data unit 2206 may be implemented as data cache <u>unit</u> 206 216 in Figure 2. In this example, each time data 2208 is accessed, counter 2210 is incremented. Data 2208 and counter 2210 are both located in a particular memory location. In these examples, a new instruction may be